CLAIMS:

1. A four terminal memory cell comprising:

a first switching device having a control terminal and first and second load terminals, a first of the load terminals being coupled to a row line;

a first load element having a first terminal coupled to the second load terminal and having a second terminal coupled to a column line;

a second switching device having a control terminal and first and second load terminals, the first load terminal of the second switching device being coupled to the control terminal of the first switching device, the second load terminal of the second switching device being coupled to a first power supply and the control terminal of the second switching device being coupled to the second load terminal of the first switching device; and

a second load element having a first terminal coupled to a second power supply and a second terminal coupled to the second load terminal of the second switching device.

2. The memory cell of claim 1, wherein the memory cell comprises an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the memory cell.

3. The memory cell of claim 1, wherein the first switching device comprises a NMOS transistor with the control terminal corresponding to a gate of the NMOS transistor, the first load electrode corresponding to a source of the NMOS transistor.

4. The memory cell of claim 1, wherein the second switching device comprises a PMOS transistor,

5. The memory cell of claim 1, wherein the first switching device corresponds to an ultrathin MOSFET of a first polarity and wherein the second switching device corresponds to an ultrathin MOSFET of a second polarity different than the first polarity.

6. The memory cell of claim 1, wherein the control electrode of the first switching device is formed from the second load element and the control electrode of the second switching device is formed from the first load element.

7. The memory cell of claim 1, wherein the first switching device corresponds to an ultrathin MOSFET of a first polarity and wherein the second switching device corresponds to an ultrathin MOSFET of a second polarity different than the first polarity, and wherein the control electrode of the first switching device is formed from the second load element and the control electrode of the second switching device is formed from the first load element.

8. A two-transistor SRAM cell comprising:

a first FET being an ultrathin FET of a first polarity type and including a gate, a source and a drain, the source being coupled to a first control line;

a second FET being an ultrathin FET of a second polarity type and including a gate, a source and a drain, the source of the second FET being coupled to the gate of the first FET, the gate of the second FET being coupled to the drain of the first FET and the source of the second FET being coupled to a first potential;

a first load device coupled between a second potential and the gate of the first FET; and

a second load device coupled between the gate of the second FET and a second control line.

9. The SRAM cell of claim 8, wherein:

the first FET is a NMOS FET; and

the second FET is a PMOS FET.

10. The SRAM cell of claim 8, wherein:

the second load device is merged with the gate of the first FET; and

the first load device is merged with the gate of the second FET.

11. The SRAM cell of claim 8, wherein the SRAM cell comprises an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM cell.

12. The SRAM cell of claim 8, further comprising:

a semiconductor substrate having a first conductivity type;

a diffusion region formed in the substrate and having a second conductivity type different than the first conductivity type;

a first dielectric pillar formed atop the diffusion region, the first FET and the second load device being formed along one side of the first dielectric pillar; and

a second dielectric pillar formed atop the substrate, the second FET and the first load device being formed along one side of the second dielectric pillar, the one side of each pillar facing the other pillar.

13. The SRAM cell of claim 8, wherein the first and second FETs comprise polycrystalline silicon.

14. The SRAM cell of claim 8, wherein the first and second load devices comprise polycrystalline material.

15. A SRAM array forming a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells, each memory cell of the plurality comprising:

a first switching device having a control terminal and first and second load terminals, a first of the load terminals being coupled to one of the plurality of row lines;

a first load element having a first terminal coupled to the second load terminal and having a second terminal coupled to one of the plurality of column lines; and

a second switching device having a control terminal and first and second load terminals, the first load terminal of the second switching device being coupled to the control terminal of the first switching device, the second load terminal of the second switching device being coupled to the first line and the control terminal of the second switching device being coupled to the second load terminal of the first switching device; and

a second load element having a first terminal coupled to the second line and a second terminal coupled to the second load terminal of the second switching device.

16. The SRAM of claim 15, wherein:

the first switching device comprises a first ultrathin transistor; and

the second switching device comprises a second ultrathin transistor.

17. The SRAM of claim 15, wherein:

the first switching device comprises a NMOS transistor; and

the second switching device comprises a PMOS transistor.

18. The SRAM of claim 15, wherein the memory cell comprises an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM.

19. The SRAM of claim 15, wherein:

the first switching device comprises a NMOS transistor wherein a gate of the NMOS transistor is merged with the second load element; and

the second switching device comprises a PMOS transistor wherein a gate of the PMOS transistor is merged with the first load element.

20. The SRAM of claim 15, wherein the first and second switching devices and the first and second load elements comprise polycrystalline material.

21. A SRAM cell having an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM cell.

22. The SRAM cell of claim 21, wherein the SRAM cell forms a portion of a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells, each SRAM cell comprising:

a first switching device having a control terminal and first and second load terminals, a first of the load terminals being coupled to one of the plurality of row lines;

a first load element having a first terminal coupled to the second load terminal and having a second terminal coupled to one of the plurality of column lines; and

a second switching device having a control terminal and first and second load terminals, the first load terminal of the second switching device being coupled to the control terminal of the first switching device, the second load terminal of the second switching device being coupled to the first line and the control terminal of the second switching device being coupled to the second load terminal of the first switching device; and

a second load element having a first terminal coupled to the second line and a second terminal coupled to the second load terminal of the second switching device.

23. The SRAM cell of claim 21, further comprising:

a first load device;

a first ultrathin transistor having a power electrode coupled to the first load device;

a second load device; and

a second ultrathin transistor including a power electrode coupled to the second load device, wherein the first load device is merged with a control electrode of the second ultrathin transistor and vice versa.

24. The SRAM of claim 21, further comprising:

a first load device;

a NMOS transistor including a power electrode coupled to the first load device;

a second load device; and

a PMOS transistor including a power electrode coupled to the second load device, wherein a gate of the NMOS transistor is merged with the second load device and a gate of the PMOS transistor is merged with the first load device.

25. A computer system comprising:

a central processing unit;

an input interface coupled to the central processing unit; and

a memory device coupled to the central processing unit, the memory device storing instructions and data for use by the central processing unit, wherein the memory device includes a SRAM array formed from cells each including in combination:

a first load device;

a first ultrathin transistor having a power electrode coupled to the first load device;

a second load device; and

a second ultrathin transistor including a power electrode coupled to the second load device, wherein the first load device is merged with a control electrode of the second ultrathin transistor and vice versa.

26. The computer system of claim 25, wherein the first ultrathin transistor comprises a vertical NMOS FET and the second ultrathin transistor comprises a vertical PMOS FET.

27. The computer system of claim 25, wherein the first transistor has a load electrode coupled to a row address line and the first load device is coupled to a column address line.

28. The computer system of claim 25, wherein the first and second transistors comprise polycrystalline semiconductor material.

29. The computer system of claim 25, wherein the first and second transistors comprise FETs each having a gate electrode, and the first load device is merged with the gate of the second transistor and the second load device is merged with the gate of the first transistor.

30. The computer system of claim 25, wherein each cell comprises an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM cell.

31. A process for forming a SRAM cell having an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM cell, the process comprising:

providing a semiconductive substrate having a first conductivity type:

forming a diffusion region of a second conductivity type different than the first conductivity type in the substrate, the diffusion region being configured to act as a row address line;

forming first and second dielectric pillars on the substrate, the first and second pillars having respective plan view areas of about F^2 and being separated by a distance of about F, one of the first and second pillars being formed atop the diffusion region and another of the first and second pillars not being formed atop the diffusion region; and

forming first and second ultrathin transistors and first and second load devices in a space between the first and second pillars, the first load device being merged with the second ultrathin transistor and the second load device being merged with the first ultrathin transistor.

32. The process of claim 31, wherein providing a semiconductive substrate comprises providing a p-type silicon substrate and wherein forming a diffusion region comprises forming an elongated n+ diffusion region configured to perform as a row address line.

33. The process of claim 31, wherein forming first and second dielectric pillars comprises forming first and second silicon dioxide pillars having a thickness of about two thousand Angstroms.

34. The process of claim 31, wherein forming first and second ultrathin transistors and first and second load devices comprises:

forming a first polycrystalline semiconductor layer on a side of the first pillar that faces the second pillar;

forming a second polycrystalline semiconductor layer on a side of the second pillar that faces the first pillar;

forming a dielectric layer on a surface of the substrate between the first and second pillars and extending upwards on an exterior surface of the first polycrystalline semiconductor layer;

forming semiconducting material atop a portion of the dielectric layer extending between the first and second pillars, the semiconducting material abutting at least a portion of the dielectric layer formed on the first polycrystalline layer, the semiconducting material abutting a portion of the second polycrystalline layer;

removing exposed portions of the dielectric layer;

forming a second dielectric layer atop the semiconducting material to extend between the first and second polycrystalline semiconductor layers and abutting a portion of the second polycrystalline layer; and

forming second semiconducting material atop the second dielectric layer and to extend between the dielectric layer and the second polycrystalline semiconductor layer.

35. The process of claim 31, wherein forming first and second dielectric pillars includes forming semiconductive material atop the first and second pillars.

36. The process of claim 31, wherein forming first and second ultrathin transistors comprises forming a PMOS FET and a NMOS FET.

37. The process of claim 31, wherein forming first and second dielectric pillars comprises anisotropic etching.

38. A process for turning a SRAM cell OFF comprising increasing a voltage applied to a switch in the SRAM cell above a threshold voltage for that switch.

39. The process of claim 38, wherein the act of turning a SRAM cell OFF comprises turning a row of SRAM cells OFF.

40. The process of claim 38, wherein the SRAM cell comprises a first transistor and a second transistor, wherein the switch comprises the second transistor and wherein the second transistor comprises an ultrathin NMOS transistor having a gate, a source, a drain and a threshold voltage, the source being coupled to a row address line and the drain being coupled to a column address line and wherein the act of turning a SRAM cell OFF comprises raising a voltage coupled to the row address line above the threshold and turning a row of SRAM cells coupled to that row address line OFF.

41. The process of claim 38, wherein the act of turning a SRAM cell OFF comprises turning OFF all of the transistors in that cell.

42. The process of claim 38, wherein the first transistor comprises an ultrathin PMOS transistor having a gate, a source and a drain and the switch comprises the second transistor, the second transistor comprising an ultrathin NMOS transistor having a gate, a source and a drain, the NMOS transistor source being coupled to a row address line and the NMOS transistor drain being coupled to a column address line and wherein the act of turning a SRAM cell OFF comprises:

raising a voltage coupled to the row address line above the threshold and turning the NMOS transistor coupled to that row address line OFF; and

causing a source-drain voltage of the PMOS transistor to become less than a threshold voltage for the PMOS transistor in response to the NMOS transistor turning OFF.

43. The process of claim 38, wherein the SRAM cell is coupled to a row address line and wherein the act of turning a SRAM cell OFF comprises raising a voltage coupled to the row address line from about zero volts to about 0.7 volts or less.

44. The process of claim 38, wherein the act of turning a SRAM cell OFF comprises turning OFF both of the two transistors in that cell.

45. A process for writing a SRAM cell comprising two switches, where one of the two switches is coupled to a row address line and a column address line, to an ON state, comprising modifying a voltage coupled to the row address line to cause a voltage applied to a control electrode of the one switch to exceed a threshold voltage for that switch.

46. The process of claim 45, further comprising modifying voltages coupled to column address lines of SRAM cells that are not to be written to the ON state to prevent the row address line voltage modification from turning ON switches in the SRAM cells that are not to be written to the ON state.

47. The process of claim 46, wherein modifying voltages coupled to column address lines comprises raising the voltages coupled to the address lines of SRAM cells that are not to be written to the ON state.

48. The process of claim 45, wherein at least one of the two switches comprises a NMOS FET having a gate, drain, source and threshold voltage V_{TN}, wherein the source is coupled to the row address line and the drain is coupled to the column address line, wherein modifying a voltage coupled to the row address line comprises reducing the voltage coupled to the row address line below ground to cause a voltage applied to the gate to exceed the threshold voltage V_{TN}.

49. The process of claim 45, further comprising, prior to modifying a voltage, writing a row of SRAM cells coupled to the row address line to the OFF state.

50. A process for reading data from a SRAM cell including a first transistor of a first conductivity type and a second transistor of a second conductivity type comprising:

increasing a voltage across a portion of the cell including two power electrodes of one of the first and second transistors; and

monitoring a current through the power electrodes of the one transistor.

51. The process of claim 50, wherein increasing comprises increasing the voltage by less than an amount represented by a turn-on voltage of the one transistor.

52. The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor and the second transistor comprises an ultrathin NMOS transistor, and wherein:

increasing comprises lowering a voltage impressed on a source of the NMOS transistor below a ground reference voltage; and

monitoring comprises monitoring a drain current of the NMOS transistor.

53. The process of claim 50, further comprising:

determining that a first logical state was stored in the SRAM cell when no current increase accompanies increasing; and

determining that a second logical state different than the first logical state was stored in the SRAM cell when a current increase accompanies increasing.

54. The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor having a gate, a source and a drain and the second transistor comprises an ultrathin NMOS transistor having a gate, a source and a drain, the NMOS transistor source being coupled to a row address line and the NMOS transistor drain being coupled to a column address line and wherein:

increasing comprises reducing a potential applied to the row address line; and

monitoring comprises monitoring a current through the column address line.

55. The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor having a gate, a source and a drain and the second transistor comprises an ultrathin NMOS transistor having a gate, a source and a drain and wherein increasing comprises increasing a gate-source voltage of the NMOS transistor to a value that is less than a threshold voltage of the NMOS transistor.